SLWK 1303.045US01
Micron 01-1139

UNITED STATES PATENT APPLICATION

ATOMIC LAYER DEPOSITION OF METAL OXIDE AND/OR LOW ASYMMETRICAL TUNNEL BARRIER INTERPLOY INSULATORS

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Cross Reference To Related Applications

This application is a Continuation-in-Part of U.S. patent application 09/943,134 filed on August 30, 2001.

This application is related to the following co-pending, commonly assigned U.S. patent applications: "DRAM Cells with Repressed Memory Metal Oxide Tunnel Insulators," attorney docket no. 1303.019US1, serial number 09/945,395, "Flash Memory with Low Tunnel Barrier Interpoly Insulators," attorney docket no. 1303.014US1, serial number 09/945,507, "Dynamic Electrically Alterable Programmable Memory with Insulating Metal Oxide Interpoly Insulators," attorney docket no. 1303.024US1, serial number 09/945,498, "Field Programmable Logic Arrays with Metal Oxide and/or Low Tunnel Barrier Interpoly Insulators," attorney docket no. 1303.027US1, serial number 09/945,512, "SRAM Cells with Repressed Floating Gate Memory, Metal Oxide Tunnel Interpoly Insulators," attorney docket no. 1303.028US1, serial number 09/945,554, "Programmable Memory Address and Decode Devices with Low Tunnel Barrier Interpoly Insulators," attorney docket no. 1303.029US1, serial number 09/945,500, and "Programmable Array Logic or Memory with P-Channel Devices and Asymmetrical Tunnel Barriers," attorney docket no. 1303.035US1, serial number 10/028,001, each of which disclosure is herein incorporated by reference.

Field of the Invention

The present invention relates generally to integrated circuits, and in particular to programmable array type logic and/or memory devices with asymmetrical low tunnel barrier interpoly insulators.

Background of the Invention

Flash memories have become widely accepted in a variety of applications ranging from personal computers, to digital cameras and wireless phones. Both INTEL and AMD have separately each produced about one billion integrated circuit chips in this technology.

The original EEPROM or EARPROM and flash memory devices described by Toshiba in 1984 used the interpoly dielectric insulator for erase. (See generally, F. Masuoka et al., "A new flash EEPROM cell using triple polysilicon technology," IEEE Int. Electron Devices Meeting, San Francisco, pp. 464-67, 1984; F. Masuoka et al., "256K flash EEPROM using triple polysilicon technology," IEEE Solid-State Circuits Conf., Philadelphia, pp. 168-169, 1985). Various combinations of silicon oxide and silicon nitride were tried. (See generally, S. Mori et al., "reliable CVD inter-poly dialectics for advanced E&EEPROM," Symp. On VLSI Technology, Kobe, Japan, pp. 16-17, 1985). However, the rough top surface of the polysilicon floating gate resulted in, poor quality interpoly oxides, sharp points, localized high electric fields, premature breakdown and reliability problems.

Widespread use of flash memories did not occur until the introduction of the ETOX cell by INTEL in 1988. (See generally, US PATENT 4,780, 424, "Process for fabricating electrically alterable floating gate memory devices," 25 Oct. 1988; B. Dipert and L. Hebert, "Flash memory goes mainstream," IEEE Spectrum, pp. 48-51, October, 1993; R. D. Pashley and S. K. Lai, "Flash memories, the best of two worlds," IEEE Spectrum, pp. 30-33, December 1989). This extremely simple cell and device structure resulted in high densities, high yield in production and low cost. This enabled the widespread use and application of flash memories anywhere a non-volatile memory function is required. However, in order to enable a reasonable write speed the ETOX cell uses channel hot electron injection, the erase operation which can be slower is achieved by Fowler-Nordhiem tunneling from the floating gate to the source. The large barriers to electron tunneling or hot electron

injection presented by the silicon oxide-silicon interface, 3.2 eV, result in slow write and erase speeds even at very high electric fields. The combination of very high electric fields and damage by hot electron collisions in the oxide result in a number of operational problems like soft erase error, reliability problems of premature oxide breakdown and a limited number of cycles of write and erase.

Other approaches to resolve the above described problems include; the use of different floating gate materials, e.g. SiC, SiOC, GaN, and GaAlN, which exhibit a lower work function (see Figure 1A), the use of structured surfaces which increase the localized electric fields (see Figure 1B), and amorphous SiC gate insulators with larger electron affinity, χ, to increase the tunneling probability and reduce erase time (see Figure 1C).

One example of the use of different floating gate (Figure 1A) materials is provided in US Patent no. 5,801,401 by L. Forbes, entitled "FLASH MEMORY WITH MICROCRYSTALLINE SILICON CARBIDE AS THE FLOATING GATE STRUCTURE." Another example is provided in US Patent no. 5,852,306 by L. Forbes, entitled "FLASH MEMORY WITH NANOCRYSTALLINE SILICON FILM AS THE FLOATING GATE." Still further examples of this approach are provided in pending applications by L. Forbes and K. Ahn, entitled "DYNAMIC RANDOM ACCESS MEMORY OPERATION OF A FLASH MEMORY DEVICE WITH CHARGE STORAGE ON A LOW ELECTRON AFFINITY GaN OR GaAIN FLOATING GATE," serial no. 08/908098, and "VARIABLE ELECTRON AFFINITY DIAMOND-LIKE COMPOUNDS FOR GATES IN SILICON CMOS MEMORIES AND IMAGING DEVICES," serial no. 08/903452.

An example of the use of the structured surface approach (Figure 1B) is provided in US Patent no. 5,981,350 by J. Geusic, L. Forbes, and K.Y. Ahn, entitled "DRAM CELLS WITH A STRUCTURE SURFACE USING A SELF STRUCTURED MASK." Another example is provided in US Patent no. 6,025, 627 by L. Forbes and J. Geusic, entitled "ATOMIC LAYER EXPITAXY GATE

INSULATORS AND TEXTURED SURFACES FOR LOW VOLTAGE FLASH MEMORIES."

Finally, an example of the use of amorphous SiC gate insulators (Figure 1C) is provided in US Patent Application serial no. 08/903453 by L. Forbes and K. Ahn, entitled "GATE INSULATOR FOR SILICON INTEGRATED CIRCUIT TECHNOLOGY BY THE CARBURIZATION OF SILICON."

Additionally, graded composition insulators to increase the tunneling probability and reduce erase time have been described by the same inventors. (See, L. Forbes and J. M. Eldridge, "GRADED COMPOSITION GATE INSULATORS TO REDUCE TUNNELING BARRIERS IN FLASH MEMORY DEVICES," application serial no. 09/945,514.

However, all of these approaches relate to increasing tunneling between the floating gate and the substrate such as is employed in a conventional ETOX device and do not involve tunneling between the control gate and floating gate through and inter-poly dielectric.

Therefore, there is a need in the art to provide improved programmable array type logic and/or memory devices while avoiding the large barriers to electron tunneling or hot electron injection presented by the silicon oxide-silicon interface, 3.2 eV, which result in slow write and erase speeds even at very high electric fields. There is also a need to avoid the combination of very high electric fields and damage by hot electron collisions in the which oxide result in a number of operational problems like soft erase error, reliability problems of premature oxide breakdown and a limited number of cycles of write and erase. Further, when using an interpoly dielectric insulator erase approach, the above mentioned problems of having a rough top surface on the polysilicon floating gate which results in, poor quality interpoly oxides, sharp points, localized high electric fields, premature breakdown and reliability problems must be avoided.

Summary of the Invention

The above mentioned problems with programmable array type logic and/or memory devices and other problems are addressed by the present invention and will be understood by reading and studying the following specification. Systems and methods are provided for programmable array type logic and/or memory devices with asymmetrical, low tunnel barrier interpoly insulators.

In one embodiment of the present invention, a non-volatile memory cell, or floating gate transistor, includes a first source/drain region and a second source/drain region separated by a channel region in a substrate. A floating gate opposes the channel region and is separated therefrom by a gate oxide. A control gate opposes the floating gate. The control gate is separated from the floating gate by an asymmetrical low tunnel barrier intergate insulator. The low tunnel barrier intergate insulator includes a metal oxide insulator selected from the group consisting of Al_2O_3, Ta_2O_5, TiO_2, ZrO_2, Nb_2O_5, $SrBi_2Ta_2O_3$, $SrTiO_3$, $PbTiO_3$, and $PbZrO_3$. The floating gate includes a polysilicon floating gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator. And, the control gate includes a polysilicon control gate having a metal layer, having a different work function from the metal layer formed on the floating gate, formed thereon in contact with the low tunnel barrier intergate insulator.

These and other embodiments, aspects, advantages, and features of the present invention will be set forth in part in the description which follows, and in part will become apparent to those skilled in the art by reference to the following description of the invention and referenced drawings or by practice of the invention. The aspects, advantages, and features of the invention are realized and attained by means of the instrumentalities, procedures, and combinations particularly pointed out in the appended claims.

Brief Description of the Drawings

Figures 1A-1C illustrate a number of previous methods for reducing tunneling barriers in Flash memory.

Figure 2 illustrates one embodiment of a floating gate transistor, or non-volatile memory cell, according to the teachings of the present invention.

Figure 3 illustrates another embodiment of a floating gate transistor, or non-volatile memory cell, according to the teachings of the present invention.

Figure 4 is a perspective view illustrating an array of silicon pillars formed on a substrate as used in one embodiment according to the teachings of the present invention.

Figures 5A-5E are cross sectional views taken along cut line 5-5 from Figure 4 illustrating a number of floating gate and control gate configurations which are included in the scope of the present invention.

Figures 6A-6D illustrate a number of address coincidence schemes can be used together with the present invention.

Figure 7A is an energy band diagram illustrating the band structure at vacuum level with the low tunnel barrier interpoly insulator according to the teachings of the present invention.

Figure 7B is an energy band diagram illustrating the band structure during an erase operation of electrons from the floating gate to the control gate across the low tunnel barrier interpoly insulator according to the teachings of the present invention.

Figure 7C is a graph plotting tunneling currents versus the applied electric fields (reciprocal applied electric field shown) for an number of barrier heights.

Figure 8 illustrates a block diagram of an embodiment of an electronic system 801 according to the teachings of the present invention.

Figure 9 is a table which provides relevant data on the barrier heights, energy gaps, dielectric constants and electron affinities of a wide variety of metal oxides that could be used as asymmetric tunnel barriers according to the teachings of the present invention.

Figure 10 illustrates a block diagram of an embodiment of an electronic system according to the teachings of the present invention.

Description of the Preferred Embodiments

In the following detailed description of the invention, reference is made to the accompanying drawings which form a part hereof, and in which is shown, by way of illustration, specific embodiments in which the invention may be practiced. The embodiments are intended to describe aspects of the invention in sufficient detail to enable those skilled in the art to practice the invention. Other embodiments may be utilized and changes may be made without departing from the scope of the present invention. In the following description, the terms wafer and substrate are interchangeably used to refer generally to any structure on which integrated circuits are formed, and also to such structures during various stages of integrated circuit fabrication. Both terms include doped and undoped semiconductors, epitaxial layers of a semiconductor on a supporting semiconductor or insulating material, combinations of such layers, as well as other such structures that are known in the art.

The term "horizontal" as used in this application is defined as a plane parallel to the conventional plane or surface of a wafer or substrate, regardless of the orientation of the wafer or substrate. The term "vertical" refers to a direction perpendicular to the horizontal as defined above. Prepositions, such as "on", "side" (as in "sidewall"), "higher", "lower", "over" and "under" are defined with respect to the conventional plane or surface being on the top surface of the wafer or substrate, regardless of the orientation of the wafer or substrate. The following detailed

description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims, along with the full scope of equivalents to which such claims are entitled.

The present invention, describes the use of asymmetrical metal oxide inter-poly dielectric insulators, formed by atomic layer deposition (ALD), between the control gate and the floating gate of non-volatile memory cells. An example is shown in Figure 2 for a planar structure, or horizontal non-volatile memory cell. This non-volatile memory cell, as described herein, can then be implemented in a number of programmable array type logic and/or memory devices according to the teachings of the present invention.

According to the teachings of the present invention. The use of an asymmetrical metal oxide films, formed by atomic layer deposition (ALD), for this purpose offer a number of advantages including:

(i) Flexibility in selecting a range of smooth metal film surfaces and compositions that can be oxidized to form tunnel barrier insulators.

(ii) Employing simple "low temperature oxidation" to produce oxide films of highly controlled thickness, composition, purity and uniformity.

(iii) Avoiding inadvertent inter-diffusion of the metal and silicon as well as silicide formation since the oxidation can be carried out at such low temperatures.

(iv) Using metal oxides that provide desirably lower tunnel barriers, relative to barriers currently used such as SiO_2.

(v) Providing a wide range of higher dielectric constant oxide films with improved capacitance characteristics.

(vi) Providing a unique ability to precisely tailor tunnel oxide barrier properties for various device designs and applications.

(vii) Permitting the use of thicker tunnel barriers, if needed, to enhance device performance and its control along with yield and reliability.

(viii) Developing layered oxide tunnel barriers by atomic layer deposition on multiple oxide layers in order, for example, to enhance device yields and reliability more typical of single insulating layers.

(ix) Eliminating soft erase errors caused by the current technique of tunnel erase from floating gate to the source.

Figure 2 illustrates one embodiment of a floating gate transistor, or non-volatile memory cell 200, according to the teachings of the present invention. As shown in Figure 2, the non-volatile memory cell 200 includes a first source/drain region 201 and a second source/drain region 203 separated by a channel region 205 in a substrate 206. A floating gate 209 opposes the channel region 205 and is separated therefrom by a gate oxide 211. A control gate 213 opposes the floating gate 209. According to the teachings of the present invention, the control gate 213 is separated from the floating gate 209 by an asymmetrical low tunnel barrier intergate insulator 215.

In one embodiment of the present invention, the asymmetrical low tunnel barrier intergate insulator 215 includes an asymmetrical metal oxide insulator which is aluminum oxide (Al_2O_3). In an alternative embodiment of the present invention, the asymmetrical low tunnel barrier intergate insulator 215 includes an asymmetrical transition metal oxide selected from the group consisting of Ta_2O_5, TiO_2, ZrO_2, and Nb_2O_5. In still another alternative embodiment of the present invention, the asymmetrical low tunnel barrier intergate insulator 215 includes an asymmetrical Perovskite oxide tunnel barrier selected from the group consisting of $SrBi_2Ta_2O_3$, $SrTiO_3$, $PbTiO_3$, and $PbZrO_3$

According to the teachings of the present invention, the floating gate 209 includes a polysilicon floating gate 209 having a metal layer 216 formed thereon in contact with the asymmetrical low tunnel barrier intergate insulator 215. Likewise, the control gate 213 includes a polysilicon control gate 213 having a metal layer 217, having a work function different from the metal layer 216 formed on the

floating gate 209, formed thereon in contact with the asymmetrical low tunnel barrier intergate insulator 215. In one embodiment, metal layer 216 is formed of the same metal material used to form the asymmetrical metal oxide interpoly insulator 215. As stated above, the non-volatile memory cell, as described herein, can then be implemented in a number of programmable array type logic and/or memory devices according to the teachings of the present invention.

Figure 3 illustrates another embodiment of a floating gate transistor, or non-volatile memory cell 300, according to the teachings of the present invention. As shown in the embodiment of Figure 3, the non-volatile memory cell 300 includes a vertical non volatile memory cell 300. In this embodiment, the non-volatile memory cell 300 has a first source/drain region 301 formed on a substrate 306. A body region 307 including a channel region 305 is formed on the first source/drain region 301. A second source/drain region 303 is formed on the body region 307. Methods for forming such a vertical transistor structure are disclosed in US Patent no. 6,135,175, entitled "Memory Address Decode Array with vertical transistors, which is incorporated herein by reference. A floating gate 309 opposes the channel region 305 and is separated therefrom by a gate oxide 311. A control gate 313 opposes the floating gate 309. According to the teachings of the present invention, the control gate 313 is separated from the floating gate 309 by an asymmetrical low tunnel barrier intergate insulator 315.

In one embodiment of the present invention, low tunnel barrier intergate insulator 315 includes an asymmetrical metal oxide insulator which is aluminum oxide (Al_2O_3). In an alternative embodiment of the present invention, the asymmetrical low tunnel barrier intergate insulator 315 includes an asymmetrical transition metal oxide selected from the group consisting of Ta_2O_5, TiO_2, ZrO_2, and

Nb_2O_5. In still another alternative embodiment of the present invention, the low tunnel barrier intergate insulator 315 includes an asymmetrical Perovskite oxide tunnel barrier selected from the group consisting of $SrBi_2Ta_2O_3$, $SrTiO_3$, $PbTiO_3$, and $PbZrO_3$.

The floating gate 309 includes a polysilicon floating gate 309 having a metal layer 316 formed thereon in contact with the asymmetrical low tunnel barrier intergate insulator 315. The control gate 313 includes a polysilicon control gate 313 having a metal layer 317, having a work function different from the metal layer 316 formed on the floating gate 309, formed thereon in contact with the asymmetrical low tunnel barrier intergate insulator 315. As stated above, the non-volatile memory cell, as described herein, can then be implemented in a number of programmable array type logic and/or memory devices according to the teachings of the present invention.

As shown in Figure 3, the floating gate 309 includes a vertical floating gate 309 formed alongside of the body region 307. In the embodiment shown in Figure 3, the control gate 313 includes a vertical control gate 313 formed alongside of the vertical floating gate 309.

As will be explained in more detail below, the floating gate 309 and control gate 313 orientation shown in Figure 3 is just one embodiment for a vertical non volatile memory cell 300, according to the teachings of the present invention. In other embodiments, explained below, the floating gate includes a horizontally oriented floating gate formed alongside of the body region. In this alternative embodiment, the control gate includes a horizontally oriented control gate formed above the horizontally oriented floating gate.

Figure 4 is a perspective view illustrating an array of silicon pillars 400-1, 400-2, 400-3, . . ., 400-N, formed on a substrate 406 as used in one embodiment according to the teachings of the present invention. As will be understood by one of ordinary skill in the art upon reading this disclosure, the substrates can be (i)

conventional p-type bulk silicon or p-type epitaxial layers on p+ wafers, (ii) silicon on insulator formed by conventional SIMOX, wafer bonding and etch back or silicon on sapphire, or (iii) small islands of silicon on insulator utilizing techniques such as described in more detail in U.S. patent no. 5,691,230, by Leonard Forbes, entitled "Technique for Producing Small Islands of Silicon on Insulator," issued 11/25/1997, which is incorporated herein by reference.

As shown in Figure 4, each pillar in the array of silicon pillars 400-1, 400-2, 400-3, . . ., 400-N, includes a first source/drain region 401 and a second source/drain region 403. The first and the second source/drain regions, 401 and 403, are separated by a body region 407 including channel regions 405. As shown in Figure 4, a number of trenches 430 separate adjacent pillars in the array of silicon pillars 400-1, 400-2, 400-3, . . ., 400-N. Trenches 430 are referenced in connection with the discussion which follows in connection with Figures 5A-5E.

Figures 5A-5E are cross sectional views taken along cut line 5-5 from Figure 4. As mentioned above in connection with Figure 3, a number of floating gate and control gate configurations are included in the present invention. Figure 5A illustrates one such embodiment of the present invention. Figure 5A illustrates a first source/drain region 501 and second source/drain region 503 for a non-volatile memory cell 500 formed according to the teachings of the present invention. As shown in Figure 5, the first and second source/drain regions, 501 and 503, are contained in a pillar of semiconductor material, and separated by a body region 507 including channel regions 505. As shown in the embodiments of Figures 5A-5E, the first source/drain region 501 is integrally connected to a buried sourceline 525. As one or ordinary skill in the art will understand upon reading this disclosure the buried sourceline 525 is be formed of semiconductor material which has the same doping type as the first source/drain region 501. In one embodiment, the sourceline 525 is formed of semiconductor material of the same doping as the first source/drain region 501, but is more heavily doped than the first source/drain region 501.

As shown in the embodiment of Figure 5A, a pair of floating gates 509-1 and 509-2 are formed in each trench 530 between adjacent pillars which form memory cells 500-1 and 500-2. Each one of the pair of floating gates, 509-1 and 509-2, respectively opposes the body regions 507-1 and 507-2 in adjacent pillars 500-1 and 500-2 on opposing sides of the trench 530.

In this embodiment, a single control gate 513 is shared by the pair of floating gates 509-1 and 509-2 on opposing sides of the trench 530. As one of ordinary skill in the art will understand upon reading this disclosure, the shared single control gate 513 can include an integrally formed control gate line. As shown in Figure 5A, such an integrally formed control gate line 513 can be one of a plurality of control gate lines which are each independently formed in the trench, such as trench 530, below the top surface of the pillars 500-1 and 500-2 and between the pair of floating gates 509-1 and 509-2. In one embodiment, according to the teachings of the present invention, each floating gate, e.g. 509-1 and 509-2, includes a vertically oriented floating gate having a vertical length of less than 100 nanometers.

As shown in the embodiment of Figure 5B, a pair of floating gates 509-1 and 509-2 are formed in each trench 530 between adjacent pillars which form memory cells 500-1 and 500-2. Each one of the pair of floating gates, 509-1 and 509-2, respectively opposes the body regions 507-1 and 507-2 in adjacent pillars 500-1 and 500-2 on opposing sides of the trench 530.

In the embodiment of Figure 5B, a plurality of control gate lines are again formed in trenches, e.g. trench 530, below the top surface of the pillars, 500-1 and 500-2, and between the pair of floating gates 509-1 and 509-2. However, in this embodiment, each trench, e.g. 530, houses a pair of control gate lines, shown as 513-1 and 513-2. Each one of the pair of control gate lines 513-1 and 513-2 addresses the floating gates, 509-1 and 509-2 respectively, on opposing sides of the trench 530. In this embodiment, the pair of control gate lines, or control gates 513-1 and 513-2 are separated by an insulator layer.

As shown in the embodiment of Figure 5C, a pair of floating gates 509-1 and 509-2 are again formed in each trench 530 between adjacent pillars which form memory cells 500-1 and 500-2. Each one of the pair of floating gates, 509-1 and 509-2, respectively opposes the body regions 507-1 and 507-2 in adjacent pillars 500-1 and 500-2 on opposing sides of the trench 530.

In the embodiment of Figure 5C, the plurality of control gate lines are disposed vertically above the floating gates. That is, in one embodiment, the control gate lines are located above the pair of floating gates 509-1 and 509-2 and not fully beneath the top surface of the pillars 500-1 and 500-2. In the embodiment of Figure 5C, each pair of floating gates, e.g. 509-1 and 509-2, in a given trench shares a single control gate line, or control gate 513.

As shown in the embodiment of Figure 5D, a pair of floating gates 509-1 and 509-2 are formed in each trench 530 between adjacent pillars which form memory cells 500-1 and 500-2. Each one of the pair of floating gates, 509-1 and 509-2, respectively opposes the body regions 507-1 and 507-2 in adjacent pillars 500-1 and 500-2 on opposing sides of the trench 530.

In the embodiment of Figure 5D, the plurality of control gate lines are disposed vertically above the floating gates. That is, in one embodiment, the control gate lines are located above the pair of floating gates 509-1 and 509-2 and not fully beneath the top surface of the pillars 500-1 and 500-2. However, in the embodiment of Figure 5D, each one of the pair of floating gates, e.g. 509-1 and 509-2, is addressed by an independent one of the plurality of control lines or control gates, shown in Figure 5D as 513-1 and 513-2.

As shown in the embodiment of Figure 5E, a single floating gate 509 is formed in each trench 530 between adjacent pillars which form memory cells 500-1 and 500-2. According to the teachings of the present invention, the single floating gate 509 can be either a vertically oriented floating gate 509 or a horizontally oriented floating gate 509 formed by conventional processing techniques, or can be

a horizontally oriented floating gate 509 formed by a replacement gate technique such as described in a copending application, entitled "Flash Memory with Ultrathin Vertical Body Transistors," by Leonard Forbes and Kie Y. Ahn, application serial no. 09/780,169. In one embodiment of the present invention, the floating gate 509 has a vertical length facing the body region 505 of less than 100 nm. In another embodiment, the floating gate 509 has a vertical length facing the body region 505 of less than 50 nm. In one embodiment, as shown in Figure 5E, the floating gate 509 is shared, respectively, with the body regions 507-1 and 507-2, including channel regions 505-1 and 505-2, in adjacent pillars 500-1 and 500-2 located on opposing sides of the trench 530. In one embodiment, the control gate 513 includes a horizontally oriented control gate 513 formed above the horizontally oriented floating gate 509.

As one of ordinary skill in the art will understand upon reading this disclosure, in each of the embodiments described above in connection with Figures 5A-5E the floating gates 509 are separated from the control gate lines, or control gates 513 with an asymmetrical low tunnel barrier intergate insulator in accordance with the descriptions given above in connection with Figure 3. The modifications here are to use tunneling through the interpoly dielectric to realize flash memory devices. The vertical devices include an extra flexibility in that the capacitors, e.g. gate oxide and intergate insulator, are easily fabricated with different areas. This readily allows the use of very high dielectric constant inter-poly dielectric insulators with lower tunneling barriers.

Figures 6A-6D illustrate that a number of address coincidence schemes can be used together with the present invention. Figure 6A illustrates a NOR flash memory array 610 having a number of non-volatile memory cells 600-1, 600-2, 600-3, using a coincidence address array scheme. For purposes of illustration, Figure 6A shows a sourceline 625 coupled to a first source/drain region 601 in each of the number of non-volatile memory cells 600-1, 600-2, 600-3. The sourceline is shown

oriented in a first selected direction in the flash memory array 610. In Figure 6A, a number of control gate lines 630 are shown oriented in a second selected direction in the flash memory array 610. As shown in Figure 6A, the number of control gate lines 630 are coupled to, or integrally formed with the control gates 613 for the number of non-volatile memory cells 600-1, 600-2, 600-3. As shown in Figure 6A, the second selected direction is orthogonal to the first selected direction. Finally, Figure 6A shows a number of bitlines 635 oriented in a third selected direction in the flash memory array 610. As shown in Figure 6A, the number of bitlines are coupled to the second source/drain regions in the number of non-volatile memory cells 600-1, 600-2, 600-3. In the embodiment shown in Figure 6A the third selected direction is parallel to the second selected direction and the number of control gate lines 630 serve as address lines. Also, as shown in Figure 6A, the flash memory array 610 includes a number of backgate or substrate/well bias address lines 640 coupled to the substrate.

Using Figure 6A as a reference point, Figures 6B-6D illustrate of top view for three different coincidence address scheme layouts suitable for use with the present invention. First, Figure 6B provides the top view layout of the coincidence address scheme described in connection with Figure 6A. That is, Figure 6B illustrates a number of sourcelines 625 oriented in a first selected direction, a number of control gate lines 630 oriented in a second selected direction, and a number of bitlines 635 oriented in a third selected direction for the flash memory array 600. As explained above in connection with Figure 6A, in this embodiment, the second and third selected direction are parallel to one another and orthogonal to the first selected direction such that the number of control gate lines 630 serve as address lines.

Figure 6C provides the top view layout of another coincidence address scheme according to the teachings of the present invention. This is, Figure 6C illustrates a number of sourcelines 625 oriented in a first selected direction, a

number of control gate lines 630 oriented in a second selected direction, and a number of bitlines 635 oriented in a third selected direction for the flash memory array 600. In the embodiment of Figure 6C, the first selected direction and the third selected direction are parallel to one another and orthogonal to the second selected direction. In this embodiment, the number of control gate lines 630 again serve as address lines.

Figure 6D provides the top view layout of yet another coincidence address scheme according to the teachings of the present invention. This is, Figure 6D illustrates a number of sourcelines 625 oriented in a first selected direction, a number of control gate lines 630 oriented in a second selected direction, and a number of bitlines 635 oriented in a third selected direction for the flash memory array 600. In the embodiment of Figure 6D, the first selected direction and the second selected direction are parallel to one another and orthogonal to the third selected direction. In this embodiment, the number of bitlines 635 serve as address lines.

As will be apparent to one of ordinary skill in the art upon reading this disclosure, and as will be described in more detail below, write can still be achieved by hot electron injection and/or, according to the teachings of the present invention, tunneling from the control gate to the floating gate. According to the teachings of the present invention, block erase is accomplished by driving the control gates with a relatively large positive voltage and tunneling from the metal on top of the floating gate to the metal on the bottom of the control gate.

Figure 7A is an energy band diagram illustrating the band structure at vacuum level with the asymmetrical low tunnel barrier interpoly insulator according to the teachings of the present invention. Figure 7A is useful in illustrating the reduced tunnel barrier off of the floating gate to the control gate and for illustrating the respective capacitances of the structure according to the teachings of the present invention.

Figure 7A shows the band structure of the silicon substrate, e.g. channel region 701, silicon dioxide gate insulator, e.g. gate oxide 703, polysilicon floating gate 705, the asymmetrical low tunnel barrier interpoly dielectric 707, between metal plates 709 and 711, and then the polysilicon control gate 713, according to the teachings of the present invention.

The design considerations involved are determined by the dielectric constant, thickness and tunneling barrier height of the asymmetrical interpoly dielectric insulator 707 relative to that of the silicon dioxide gate insulator, e.g. gate oxide 703. The tunneling probability through the interpoly dielectric 707 is an exponential function of both the barrier height and the electric field across this dielectric.

Figure 7A shows the asymmetrical tunnel barriers, formed by atomic layer deposition (ALD), used for easy erase. Erase is achieved by the use of positive control gate voltages through the low tunnel barrier. In one embodiment, according to the teachings of the present invention, read utilizes positive control gate voltages with n-channel enhancement mode devices as described in the above referenced, copending applications, by the same inventors, entitled "FLASH MEMORY DEVICES WITH METAL OXIDE AND/OR LOW TUNNEL BARRIER INTERPLOY INSULATORS," attorney docket number 1303.014US1, application serial no. 09/945,507, "PROGRAMMABLE MEMORY ADDRESS AND DECODE DEVICES WITH METAL OXIDE AND/OR LOW TUNNEL BARRIER INTERPLOY INSULATORS," attorney docket number 1303.029US1, application serial no. 09/945,500, "FIELD PROGRAMMABLE LOGIC ARRAYS WITH METAL OXIDE AND/OR LOW TUNNEL BARRIER INTERPLOY INSULATORS, attorney docket number 1303.027US1, application serial no. 09/945,512, "DEAPROM WITH INSULATING METAL OXIDE INTERPLOY INSULATORS," attorney docket number 1303.024US1, application serial no. 09/945,498. In another embodiment, according to the teachings of the present invention, read utilizes negative control gate voltages with n-channel depletion

mode devices as described in the above referenced, copending application, by the same inventors, entitled "PROGRAMMABLE ARRAY TYPE LOGIC AND/OR MEMORY DEVICES WITH METAL OXIDE AND/OR LOW ASYMMETRICAL TUNNEL BARRIER INTERPLOY INSULATORS," attorney docket number 1303.020US1, application serial no. 09/943,134. In another embodiment, according to the teachings of the present invention, read utilizes negative control gate voltages with p-channel enhancement mode devices as described in the above referenced, copending application, by the same inventors, entitled "PROGRAMMABLE ARRAY TYPE LOGIC OR MEMORY WITH P-CHANNEL DEVICES AND ASYMMETRICAL TUNNEL BARRIERS," attorney docket number 1303.035US1, application serial no. 10/028,001. Programming is accomplished by channel hot electron injection with n-channel devices and/or electron injection from the control gate for both n-channel and p-channel devices and may or may not utilize positive substrate, well, or body bias.

Figure 7B is an energy band diagram illustrating the band structure during an erase operation of electrons from the floating gate 705 to the control gate 713 across the low tunnel barrier interpoly insulator 707 according to the teachings of the present invention. Figure 7B is similarly useful in illustrating the reduced tunnel barrier off of the floating gate 705 to the control gate 713 and for illustrating the respective capacitances of the structure according to the teachings of the present invention.

As shown in Figure 7B, the electric field is determined by the total voltage difference across the structure, the ratio of the capacitances (see Figure 7A), and the thickness of the asymmetrical interpoly dielectric 707. The voltage across the asymmetrical interpoly dielectric 707 will be, $\Delta V2 = V\ C1/(C1 + C2)$, where V is the total applied voltage. The capacitances, C, of the structures depends on the dielectric constant, ϵ_r, the permittivity of free space, ϵ_o, and the thickness of the insulating layers, t, and area, A, such that $C = \epsilon_r\ \epsilon_o\ A/t$, Farads/cm^2, where ϵ_r is the

low frequency dielectric constant. The electric field across the asymmetrical interpoly dielectric insulator 707, having capacitance, C2, will then be E2 = ΔV2/t2, where t2 is the thickness of this layer.

The tunneling current in erasing charge from the floating gate 705 by tunneling to the control gate 713 will then be as shown in Figure 7B given by an equation of the form:

$$J = B \exp(- Eo/E)$$

where E is the electric field across the interpoly dielectric insulator 707 and Eo depends on the barrier height. Practical values of current densities for aluminum oxide which has a current density of 1 A/cm^2 at a field of about E = 1V/20Å = $5x10^{+6}$ V/cm are evidenced in a description by Pollack. (See generally, S. R. Pollack and C. E. Morris, "Tunneling through gaseous oxidized films of Al_2O_3," Trans. AIME, Vol. 233, p. 497, 1965). Practical current densities for silicon oxide transistor gate insulators which has a current density of 1 A/cm^2 at a field of about E = 2.3V/23A = $1x10^{+7}$ V/cm are evidenced in a description by T. P. Ma et al. (See generally, T. P. Ma et al., "Tunneling leakage current in ultrathin (< 4 nm) nitride/oxide stack dielectrics," IEEE Electron Device Letters, vol. 19, no. 10, pp. 388-390, 1998).

The lower electric field in the aluminum oxide interpoly insulator 707 for the same current density reflects the lower tunneling barrier of approximately 2 eV, shown in Figure 7B, as opposed to the 3.2 eV tunneling barrier of silicon oxide 703, also illustrated in Figure 7B.

Figure 7C is a graph plotting tunneling currents versus the applied electric fields (reciprocal applied electric field shown) for a number of barrier heights. Figure 7C illustrates the dependence of the tunneling currents on electric field (reciprocal applied electric field) and barrier height. The fraction of voltage across the asymmetrical interpoly or asymmetrical intergate insulator, ΔV2, can be increased by making the area of the intergate capacitor, C2, (e.g. intergate insulator

707) smaller than the area of the transistor gate capacitor, C1 (e.g. gate oxide 703). This would be required with high dielectric constant intergate dielectric insulators 707 and is easily realized with the vertical floating gate structures described above in connection with Figures 3, and 5A-5E.

Methods of Formation

As described above, this disclosure describes the use of asymmetrical tunnel barriers formed by atomic layer deposition (ALD) and specifically low tunnel barriers during erase, to make erase of flash memory type devices easier. In conventional flash memory type devices with tunnel erase from the floating gate to the transistor source, the silicon oxide presents a very high 3.2 eV barrier and high electric fields are required. The combination of very high electric fields and damage by hot electron collisions in the oxide result in a number of operational problems like soft erase error, reliability problems of premature oxide breakdown and a limited number of cycles of write and erase. The tunneling currents depend exponentially on the barrier heights. An asymmetrical barrier, as shown in Figure 7A, presents a low barrier for erase but can present a higher barrier during read and/or write operations when tunneling is not desired. These asymmetrical barriers can be achieved various ways, one technique is to use different metal contact plates, with the upper plate on the interpoly or intergate insulator being a metal like platinum with a large work function as described above in the referenced, copending application, by the same inventors, entitled "PROGRAMMABLE ARRAY LOGIC OR MEMORY DEVICES WITH ASYMMETRICAL TUNNEL BARRIERS," attorney docket number 1303.020US1, application serial number 09/943,134.

Key characteristics of ultra-thin ALD oxides for this invention include the following:

(a) Films can be grown at low (<300 to 400 degrees Celsius) temperatures.

(b) Films can be grown on a variety of substrate materials, including a wide range of inorganic (e.g., silicon, glass, oxide and nitride) to metallic surfaces.

(c) Films can be comprised of single (e.g., Al_2O_3) and multiple metal components.

(d) The thicknesses of the oxide films can be controlled to within a thickness of 1 monolayer. Their thickness uniformities are exceptionally high.

(e) Films are chemically homogeneous, uniform and have a strong tendency to form the most stable compositions in their respective metal-oxygen systems. For example, Ta_2O_5 forms in the Ta-O system.

(f) Even ultra-thin films exhibit excellent step and sidewall coverage. This will be particularly advantageous for enhancing the quality of so-called "vertical transistor" devices. Step coverage difficulties are relatively less demanding in "horizontally configured" transistors.

(g) Control of the bottom metal layer thickness and uniformity are less demanding, provided the metal is sufficiently conductive throughout. In other words, the prime function of the metal, in combination with the appropriate oxide, is to produce a lower tunnel barrier relative to conventional barriers such as Si/SiO_2.

(h) Films are excellent insulators with high breakdown strengths.

(i) Films have high dielectric constants as formed at low temperatures. This invention does not require that the oxides have very high dielectric constants. However, if necessary, many of the ALD oxides can be subsequently heat treated to substantially increase their dielectric constants. Such changes typically result from minute

micro-structural changes, i.e., transformations from amorphous to nano-crystalline phases.

As is well-known to those in the field, the literature describing ALD oxide processes is quite large and still expanding rapidly. Within reasonable constraints imposed by chemical and physical properties of component metals and their oxides, ALD processes can be developed for producing an even wider range of single and multi-component oxide thin films. A few examples of ALD processes for forming some useful oxides for tunnel barriers and other applications are given next.

Al_2O_3 Films. A variety of ALD processes have been described for making high quality, ultra-thin Al_2O_3 films. Thus Kim et al. (see generally, Y.K. Kim et al., "Novel capacitor technology for high density, stand-alone and embedded DRAMs", IEDM (2000)) describe the use of TMA and ozone to form superior Al_2O_3 films on silicon at 350C for DRAM applications. J. H. Lee et al. (see generally, J.H. Lee, et al., "Effect of polysilicon gate on the flatband voltage shift and mobility degradation for ALD-Al_2O_3 gate dielectric", IEDM (2000); D-G Park et al., "Characteristics of n^+ polycrystalline-Si/Al_2O_3/Si metal-oxide-semiconductor structures prepared by atomic layer chemical vapor deposition using $Al(Ch_3)_3$ and H_2O vapor", Jour. Appl. Phys. **89** (11), pp. 6275-6280 (2001)) from the same laboratory investigated the effects of doped poly-silicon gate electrode layers on the properties of Al_2O_3 films formed by ALD at 450 degrees Celsius and crystallized at 850 degrees Celsius and found that interfacial dopant segregation can improve capacitive characteristics. In quite a different application, Paranjpe et al. (see generally, A. Paranjpe et al., "Atomic layer deposition of AlO_x for thin film head gap applications", Jour. Electrochem. Soc. **148** (9), G465-G471 (2001)) developed an ALD process (using TMA to form Al precursor layers and oxidizing them with water) to produce excellent AlO_x layers at 150-200 degrees Celsius for use in advanced gap and tunnel junction devices. Alumina films, grown on substrates as diverse as Si, Ta and NiFe were amorphous, conformal, stoichiometric (to within 2 at. %, pure (<5 at. %

hydrogen and <1 at. % other impurities), smooth (R_A~2 angstroms) with controllable levels of stress. Extraordinary levels of thickness control (to within 1 angstrom) have been achieved upon using ALD to form ultra-thin Al_2O_3 and SiO_2 films on BN particles. Such oxide coatings can be employed to modify surface energies in order to increase loading of BN particles in polymer films for packaging. (See generally, J.D. Ferguson et al., "Atomic layer deposition of Al_2O_3 and SiO_2 on BN particles using sequential surface reactions", Appl. Surf. Sci. **162-163**, pp. 280-292 (2000)).

Transition Metal (TM) Oxide Films. Various ALD processes have also been described for producing ultra-thin Ta_2O_5 films. Kim et al. (see generally, Y.S. Kim et al., "Effect of rapid thermal annealing on the structure and the electrical properties of atomic layer deposited Ta_2O_5 films", Jour. Korean Phys. Soc. **37** (6), pp. 975-979 (2000)) have grown such oxide films on Si wafers and ITO glasses at 300 degrees Celsius by reacting $Ta(OEt)_5$ and water. Films made under 550 degrees Celsius were amorphous. Their dielectric constant increased with RTA temperature. With increasing RTA temperatures, leakage initially became smaller and then increased as crystallization became more evident. Such effects are known to depend upon RTA ambients and Ta_2O_5 underlayers and must be optimized according to applications to produce useful tunnel barriers.

Smith et al. (see generally, R.C. Smith et al., "Chemical vapour deposition of the oxides of titanium, zirconium and hafnium for use as high-k materials in microelectronic devices. A carbon-free precursor for the synthesis of hafnium dioxide", Advanced Materials for Optics and Electronics, **10**, pp. 105-114 (2001)) surveyed Group IV metal precursors used for the formation of thin TiO_2, ZrO_2 and HfO_2 films by both CVD and ALCVD processes in an effort to produce oxides that are completely carbon-, hydrogen- and halogen-free. They found, for example, that $Hf(NO_3)_4$ could be used for making CVD HfO_2 films on silicon at temperatures as low as 300 degrees Celsius. Such films contain excess oxygen and that can

apparently be removed by heating in nitrogen at higher temperatures. Similar findings were made forming TiO_2 and ZrO_2 films. The authors opine that these oxides could be made by ALCVD, using Group IV nitrate precursors. Due to the low ALD operable temperatures, it is possible to conduct detailed *in situ* deposition rate studies in many instances in order to more precisely define metal oxide thicknesses. For example, Aarik et al. (see generally, J. Aarik et al, "Anomalous effect of temperature on atomic layer deposition of titanium dioxide", Jour. Crystal Growth **220**, pp. 531-537 (2000). See also K. Kukli et al., "Real time monitoring in atomic layer deposition of TiO_2 from TiI_4 and H_2O-H_2O_2", Langmuir **16**, pp. 8122-8128 (2000)) used a $TiCl_4 + H_2O$ ALD process to grow TiO_2 films on quartz QCM substrates: deposition rate, refractive index and related properties were highly dependent on deposition temperature in the 150 to 225 degrees Celsius range. This unexpected high dependency resulted from unusual surface roughening due to the simultaneous formation of amorphous and crystalline TiO_2 phase at the higher temperatures. Other crystalline TiO_2 phases can co-deposit at the ALD temperatures are raised to 300 to 400 degrees Celsius. Arrik et al. (see generally, J. Aarik et al., "Texture development in nanocrystalline hafnium dioxide thin films grown by atomic layer deposition", Jour. Crystal Growth **220**, pp. 105-113 (2000)) have also investigated a broader range of temperature effects on HfO_2 formed on SiO_2 and Si by ALD. Using $HfCl_4$ and H_2O as precursors, they found that amorphous films were formed at 225 degrees Celsius but crystalline films were formed at 300 degrees Celsius and above. Oxide films grown for microelectronic applications should desirably be amorphous in order to avoid porosity and grain boundaries causing high leakage currents (see generally, K. Kukli et al., "Atomic layer deposition of zirconium oxide from zirconium tetraiodide, water and hydrogen peroxide", Jour. Crystal Growth **231**, pp. 262-272 (2001)). Zirconium dioxide films have attractively high dielectric constants but generally low breakdown values due, presumably, to their strong tendency to crystallize. The results of Kukli et al.

suggest that ALD temperatures under 250 degrees Celsius should yield the desired amorphous structure when using a ZrI_4 precursor.

It has been shown that mixtures of transition metal oxides can also be deposited for use as tunnel barriers. Such processes involve depositing transition metal alloy precursor layers followed by oxidation, followed again by addition of the alloy precursor layer and so on until the desired mixed oxide tunnel junction thickness is reached. Likewise it has been shown that certain perovskite oxide oxide films can be formed by first using ALD to form the desired amorphous oxide composition and then heating to produce the perovskite crystal structure. Clearly formation of such mixed oxide films is more complex and will not be described here.

PROCESS DESCRIPTIONS

Two examples, according to the present invention, are sketched out below for building asymmetrical Metal/ALD Oxide/Metal tunnel barriers over poly-Si floating gate electrodes. Additional background and fabrication details are in earlier disclosures, as referenced herein, dependent on the particular ALD systems employed and is otherwise available to those skilled in the art. If patterning and other processes do not impose constraints, one could use an ALD system that is modified by the addition of a second processing chamber for depositing *in situ* the bottom and top metal layers. This multichamber system would provide improved control over key oxide tunnel barrier properties, especially thickness, composition and interfacial impurities.

Example I. Formation of $Al/Al_2O_3/Al$ tunnel barriers can be built having a barrier height of about ~2 eV. Figure 8 graphically illustrates the dependence of the barrier height for current injection on the work function and electron affinity of a given, homogeneous dielectric film. Figure 9 is a table which provides relevant data

on the barrier heights, energy gaps, dielectric constants and electron affinities of a wide variety of metal oxides that could be used as asymmetric tunnel barriers according to the teachings of the present invention. (See generally, H.F. Luan et al., "High quality Ta2O5 gate dielectrics with Tox equil. 10 Angstroms," IEDM Tech. Digest, pp. 141-144, 1999; J. Robertson et al., "Schottky barrier heights of tantalum oxide, barium strontium titanate, lead titanate and strontium bismuth tantalate," App. Phys. Lett., Vol. 74, No. 8, pp. 1168-1170, Feb. 1999; J. Robertson, "Band offsets of wide-band-gap oxides and implications for future electronic devices," J. Vac. Sci. Technol. B, Vol. 18, No. 3, pp. 1785-1791, 2000; Xin Guo et al., "High quality ultra-thin (1.5 nm) TiO2/Si3N4 gate dielectric for deep submicron CMOS technology," IEDM Tech. Digest, pp. 137-140, 1999; H.-S. Kim et al., "Leakage current and electrical breakdown in metal-organic chemical vapor deposited TiO2 dielectrics on silicon substrates," Appl. Phys. Lett., Vol. 69, No. 25, pp. 3860-3862, 1996; J. Yan et al., "Structure and electrical characterization of TiO2 grown from titanium tetrakis-isoproxide (TTIP) and TTIP/H2O ambient," J. Vac. Sci. Technol. B, Vol. 14, No. 3, pp. 1706-1711, 1966).

Neglecting patterning steps along the way, the processing sequence can be:

(i) Use a low energy, inert ion plasma in the auxiliary chamber to sputter clean residual oxides, etc. from the poly-Si surfaces previously fabricated on the device wafer.

(ii) Deposit an aluminum contact layer over the poly-Si. This layer is presumably ten to hundreds of angstroms thick, as needed to insure good coverage of the poly-Si.

(iii) Transfer the device wafer to the ALD processing chamber under a vacuum sufficient to prevent inadvertent oxidation.

(iv) Produce the desired Al_2O_3 layer via an ALD. Several precursor chemistries are available, as indicated by the few examples in the references cited above in connection with the discussion on Al_2O_3.

For example, the low temperature process described by Paranjpe et al. (see generally, A. Paranjpe et al., "Atomic layer deposition of AlO_x for thin film head gap applications", Jour. Electrochem. Soc. **148** (9), G465-G471 (2001)) looks attractive for this purpose since it was developed to operate at temperatures in the 150-200 degrees Celsius range, using trimethylaluminum and water as precursors. As such, Al_2O_3 films as thin as 5 to 10 Angstroms have been shown to be continuous with excellent insulating properties.

(v) Transfer the device wafer back to the auxiliary chamber and deposit the top aluminum electrode layer.

(vi) Remove the wafer from the system for further processing, e.g., addition of silicon control layer, patterning, etc.

Barriers of Al_2O_3 formed on Al will exhibit some minor barrier height difference when injecting electrons from the inner and outer electrodes. The barrier height difference will be at most 0.1 eV and will arise from small differences in oxide composition at the interfaces. (See generally copending application, entitled "PROGRAMMABLE ARRAY TYPE LOGIC OR MEMORY WITH P-CHANNEL DEVICES AND ASYMMETRICAL TUNNEL BARRIERS," attorney docket number 1303.035US1, application serial no. 10/028,001, for a complete explanation). Moreover, such small differences will not interfere with the proper functioning of the devices of this disclosure.

Example II. Formation of Al/Ta_2O_5/Al tunnel barriers can be formed with a barrier height of about 2 eV. See Figures 8 and 9. Again, processes for producing ultra-thin films of Ta_2O_5 that are suitable for tunnel barriers are known. See, for example, the work of Kim et al. (see generally, Y.S. Kim et al., "Effect of rapid thermal annealing on the structure and the electrical properties of atomic layer deposited Ta_2O_5 films", Jour. Korean Phys. Soc. **37** (6), pp. 975-979 (2000)) cited

above. Note that it may not be necessary to maximize the dielectric constant of this oxide for the present applications although such maximization is desirable for building useful, minimal area DRAM storage capacitors. One can fabricate these $Al/Ta_2O_5/Al$ tunnel barriers following the approach sketched out above.

(i) Use a low energy, inert ion plasma in the auxiliary chamber to sputter clean residual exodies, etc. from the poly-Si surfaces previously fabricated on the device wafer.

(ii) Deposit an aluminum contact layer over the poly-Si. This layer is presumably ten to hundreds of angstroms thick, as needed to insure good coverage of the poly-Si.

(iii) Transfer the device wafer to the ALD processing chamber, under a vacuum sufficient to prevent inadvertent oxidation.

(iv) Produce the desired Ta_2O_5 layer via an ALD process such as the one just cited, using a $Ta(OEt)_5$ and water as precursors and a temperature of 300 degrees Celsius or lower, if possible, in order to prevent inadvertent Al recrystallization and growth. Formed in this way, the dielectric constant of the oxide will be approximately 22-24.

(v) Transfer the device wafer back to the auxiliary chamber and deposit the top aluminum electrode layer.

(vi) Remove the wafer from the system for further processing, e.g., addition of silicon control layer, patterning, etc.

A very limited intermixing of Al and Ta oxides at the ALD formed interface can develop unless a few steps are taken to minimize this. For example, minimization of the ALD process temperature. Alternatively, first forming a monolayer of Al_2O_3 by exposing the water precursor before the $Ta(OEt)_5$ precursor. Intermixing of a monolayer or two at this interface can also be accepted (provided it is reproducible from wafer-to-wafer, run-to-run, etc.). More detailed studies have shown that the tunnel current-barrier thickness characteristics are better described in

terms of an "average barrier height." Clearly the large bulk, if not all, of the tunnel barrier will consist of a layer of Ta_2O_5 with a thickness that could lie in the range of perhaps 20 to 50 Angstroms or more. Upon reflection of a variety of metal/oxide tunnel barriers, it is evident that "nature abhors perfect interfaces." Even in the Si/SiO_2 system which is perhaps the one that approaches most nearly to perfection.

System Level

Figure 10 illustrates a block diagram of an embodiment of an electronic system 1001 according to the teachings of the present invention. In the embodiment shown in Figure 10, the system 1001 includes a memory device 1000 which has an array of memory cells 1002, address decoder 1004, row access circuitry 1006, column access circuitry 1008, control circuitry 1010, and input/output circuit 1012. Also, as shown in Figure 10, the circuit 1001 includes a processor 1014, or memory controller for memory accessing. The memory device 1000 receives control signals from the processor 1014, such as WE*, RAS* and CAS* signals over wiring or metallization lines. The memory device 1000 is used to store data which is accessed via I/O lines. It will be appreciated by those skilled in the art that additional circuitry and control signals can be provided, and that the memory device 1000 has been simplified to help focus on the invention. At least one of the processor 1014 or memory device 1000 has a memory cell formed according to the embodiments of the present invention. That is, at least one of the processor 1014 or memory device 1000 includes an asymmetrical low tunnel barrier interpoly insulator according to the teachings of the present invention.

It will be understood that the embodiment shown in Figure 10 illustrates an embodiment for electronic system circuitry in which the novel memory cells of the present invention are used. The illustration of system 1001, as shown in Figure 10, is intended to provide a general understanding of one application for the structure and circuitry of the present invention, and is not intended to serve as a complete

description of all the elements and features of an electronic system using the novel memory cell structures. Further, the invention is equally applicable to any size and type of memory device 1000 using the novel memory cells of the present invention and is not intended to be limited to that described above. As one of ordinary skill in the art will understand, such an electronic system can be fabricated in single-package processing units, or even on a single semiconductor chip, in order to reduce the communication time between the processor and the memory device.

Applications containing the novel memory cell of the present invention as described in this disclosure include electronic systems for use in memory modules, device drivers, power modules, communication modems, processor modules, and application-specific modules, and may include multilayer, multichip modules. Such circuitry can further be a subcomponent of a variety of electronic systems, such as a clock, a television, a cell phone, a personal computer, an automobile, an industrial control system, an aircraft, and others.

CONCLUSIONS

Asymmetrical low barrier tunnel insulators are described between the floating gate and control gate in a flash memory type devices to form programmable array logic and memory devices. The asymmetrical low barrier insulators, ~2.0 eV, are formed by atomic layer deposition (ALD). While the amount of charge stored on the floating gate is small the transistor provides gain and charge multiplication resulting in a large output signal and ease of reading the stored data. If there is an adverse capacitance ratio due to a large difference of dielectric constants then the vertical gate structures described previously can be employed.

It has been shown that the asymmetrical low tunnel barrier interpoly insulators of the present invention avoid the large barriers to electron tunneling or hot electron injection presented by the silicon oxide-silicon interface, 3.2 eV, which result in slow write and erase speeds even at very high electric fields. The present

invention also avoids the combination of very high electric fields and damage by hot electron collisions in the which oxide result in a number of operational problems like soft erase error, reliability problems of premature oxide breakdown and a limited number of cycles of write and erase. Further, the asymmetrical low tunnel barrier interploy dielectric insulator erase approach, of the present invention remedies the above mentioned problems of having a rough top surface on the polysilicon floating gate which results in, poor quality interpoly oxides, sharp points, localized high electric fields, premature breakdown and reliability problems.

The use of ALD greatly increases the capability of forming a given metal oxide insulator on a dissimilar metal contact layer. This ability provides a much increased latitude in independently selecting chemically and physically superior contact metals and ALD metal oxides combinations. Judicious selection of the contact metal/ALD oxide couple also provides flexibility in setting the electron tunneling barrier height over ranges not possible via the thermal oxidation approach. This dissimilar contact metal may also function as a diffusion barrier. This may be required when high temperature treatments are used subsequently to increase the dielectric constant of the oxide.

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiment shown. This application is intended to cover any adaptations or variations of the present invention. It is to be understood that the above description is intended to be illustrative, and not restrictive. Combinations of the above embodiments, and other embodiments will be apparent to those of skill in the art upon reviewing the above description. The scope of the invention includes any other applications in which the above structures and fabrication methods are used. The scope of the invention should be determined with reference to the appended claims, along with the full scope of equivalents to which such claims are entitled.